

CLAIMS

What is claimed is:

1. An integrated circuit, comprising:
 - a plurality of switches;
 - a first conductor having a first span along a first dimension, wherein the first conductor selectively couples to at least one input of each of at least two adjacent program controlled cells through a respective switch of the plurality of switches without requiring traversal of another conductor;
 - a second conductor and a third conductor having two different spans in the first dimension, wherein the first conductor selectively couples to the second conductor and the third conductor; and
 - a fourth conductor and a fifth conductor having two different spans in a second dimension, wherein each of the fourth conductor and the fifth conductor drives the first conductor through a respective independently controlled switch of the plurality of switches.
2. The integrated circuit of claim 1, wherein each of the plurality of switches comprises at least a program controlled passgate.

3. The integrated circuit of claim 1, wherein each of the plurality of switches comprises at least a program controlled driver/receiver.

4. The integrated circuit of claim 1, wherein the plurality of switches comprise at least one of a program controlled passgate and a program controlled driver/receiver.

5. The integrated circuit of claim 1, wherein one of the plurality of switches has a program controlled on state and off state.

6. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating memory devices.

7. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

8. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

9. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

10. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating Ferro-electric devices.

11. A method of operating an integrated circuit, comprising:

providing a plurality of switches;

providing a first conductor having a first span along a first dimension;

selectively coupling the first conductor to at least one input of each of at least two adjacent program controlled cells through a respective switch of the plurality of switches without requiring traversal of another conductor;

providing a second conductor and a third conductor having two different spans in the first dimension;

selectively coupling the first conductor to the second conductor and the third conductor;

providing a fourth conductor and a fifth conductor having two different spans in a second dimension; and

driving the first conductor using each of the fourth and the fifth conductors through a respective independently controlled switch of the plurality of switches.

12. The method of claim 11, wherein each of the plurality of switches comprises at least a program controlled passgate.

12. The method of claim 11, wherein each of the plurality of switches comprises at least a program controlled driver/receiver.

13. The method of claim 11, wherein the plurality of switches comprise at least one of a program controlled passgate and a program controlled driver/receiver.

14. The method of claim 11, wherein one of the plurality of switches has a program controlled on state and off state.

15. The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating memory devices.

16. The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

17. The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

18. The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

19. The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating Ferro-electric devices.